International Journal of Advance Engineering and Technology
Volume 1 Nomor 2 November 2025
e-ISSN: 3089-767X; p-ISSN:3089-8439, Page 34-55
DOI: https://doi.org/10.63956/ijaetech.v1i2.31
Available online at: https://ijaetech.org/index.php/ijaetech/article/view/30

Design and Implementation of Multiplier-Free Dual-Mode CORDIC Based DDC

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Abstract.
Digital Down Conversion (DDC) is a fundamental process in software defined radio (SDR) and digital communications, which transforms intermediate frequency (IF) signals into baseband signals. In conventional DDC designs, multipliers and look-up tables are generally employed, both of which tend to increase hardware size and power consumption. In this paper we present a Dual-Mode CORDIC-Based DDC architecture which uses the CORDIC (Coordinate Rotation Digital Computer) algorithm to eliminate multipliers. This novel architecture combines a CORDIC-based Numerically Controlled Oscillator (NCO), a CORDIC mixer, and a Cascaded Integrator-Comb (CIC) filter with a finite impulse response (FIR) com pentation filter. The NCO provides two precision modes - an 8-stage low-latency mode for speed and a 16-stage high precision mode for accuracy, giving runtime reconfigurability according to design requirements. Simulations and analysis show that the design gives highly accurate frequency translation, is efficient in hardware utilization and fully eliminates the use of digital signal processing (DSP) blocks. Overall, the architecture proposed offers a low-power, low-cost, and recon figural solution ideal for modern SDR-based applications and flexible digital signal processing systems.

Keywords: *CORDIC Algorithm, CIC Filter, Digital Down-conversion, Fixed-Point Arithmetic, Multiplier-Free Design*

INTRODUCTION

The superheterodyne receiver has been an important design applied in communications for nearly a century. The primary role of the superheterodyne receiver is to convert high-frequency Radio Frequency (RF) signals to an IF level, where further processing like filtering, demodulation, and signal analysis can be carried out relatively easily [1], [14]. With advances in SDR and DSP, the traditional analog intermediate-frequency chain is being supplanted by its digital counterpart the DDC stage [18], [20].

Digital down conversion in a superheterodyne receiver involves down converting the digitized IF signal to baseband using numerically generated sine and cosine carriers. There are three large pieces of hardware required in this process: an NCO [4],[9], digital mixer, and decimation filter [18]. Conventional DDC implementations do employ

Received: November 19, 2025; Accepted: December 20, 2025; Published: December 24, 2025
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multipliers and look-up tables (LUTs) [18], power-hungry components and hardware resources in FPGAs [5]. For high-performance SDR and Field Programmable Gate Array (FPGA) implementations, multiplier resources are the bottlenecks in performance in most cases [16], especially when reconfigurable or multi-channel operation must be supported.

To avoid these issues, the idea proposed here is a Dual-Mode CORDIC-Based Digital Down Conversion System for a super heterodyne receiver [18]. The CORDIC algorithm replaces the traditional multipliers with shift-and-add operations [6], [24] very economically, thereby reducing hardware significantly without sacrificing high accuracy. The double-mode architecture allows the system to be operated in either an 8-stage low-latency mode or a 16-stage high-precision mode, which provides dynamic tradeoffs among speed, accuracy, and power consumption [18], [17].

The design is developed using Scilab and Xilinx ISE design tools. The Scilab is employed in algorithm verification, fixed point simulation [25], and filter design, whereas the Xilinx ISE is employed in hardware synthesis, timing simulation, and power estimation [5], [3], [26]. Scilab-based modeling and Xilinx ISE verification is utilized to validate that the system achieves accurate frequency translation, low power consumption, and area minimization.

Thus, the system described here is a novel reconfigurable and high-speed DDC system that is a blend of the most advanta geous aspects of analog superheterodyne receivers and adaptive digital SDR architectures [17] in attempting to facilitate multiplier-free operation [16] to benefit future communication systems.

LITERATURE REVIEWS

2.1 CLASSIC DIGITAL DOWN CONVERSION ARCHITECTURES:

Traditional DDC architectures consist of a sophisticated chain of building blocks, i.e., NCO, digital mixer, and multi-stage decimation filters (most typically CIC or FIR filters cascaded together) [18], [5]. Execution of the key functional building blocks typically depends on the extensive use of hardware multipliers and large counts of LUTs for the mixer and phase-to amplitude conversion [18], [5].

Such reliance ultimately manifests as significant drawbacks in modern hardware platforms. Legacy architectures are con stantly power- and silicon-area-hungry and thus resource-inefficient for SDR and FPGA-based embedded systems [18], [5]. The ubiquity

of multipliers results in an initial bottleneck in high-speed environments, restricts scalability, and precludes multi-channel or reconfigurable DDC structure design due to high utilization of specialized DSP blocks [16], [13]. While other polynomial and LUT-based approximations of transcendental functions do exist, they are normally memory-hungry or still multiplier-dependent, respectively [23], [24].

CORDIC: A Multiplier-Free Building Block For Dsp

To preclude the hardware multiplier constraints in practice, digital signal processing based on CORDIC was used [23]. CORDIC is effective in the evaluation of complicated trigonometric, hyperbolic, and other transcendental functions via substitution of costly multiplications with more affordable hardware-efficient iterative shift-and-add operations [24], [6], [26]. The built-in multiplier-free properties have made CORDIC more suitable for low-power [12], low-area [12], [7], and reconfigurable computing blocks [10], [17].

The Waveform Generation (NCO) CORDIC easily surpassed the prior ROM techniques and provided a new generation of low-cost sinusoid generators [3], [24]. CORDIC is extensively used in FPGA sinusoid generators [3] and pipelined NCO's [4], [9] so that high-speed, real-time frequency synthesis can be accomplished utilizing high resolution with little resource and power loss compared to conventional LUT based NCOs [4].

Specialized Functions

The universal nature of the algorithm lends itself to specialized mathematical functions necessary in digital receivers such as high-precision calculations of arcsine and arccosine [8], [11], non-linear activation functions (for example, sigmoid and concave for edge machine learning) [12], and power functions [25].

CORDIC and DDC Implementation Advances

Research has consistently concentrated on CORDIC architectural improvements in order to overcome its principal disad vantage i.e. its high latency amongst its other faults due to its iterative nature [23], [26].

Speed and Latency

In order to increase the speed of computation, measures include low-latency application implementation on simple equa tions [22] and pipeline implementations of CORDIC [4], [9], [24] and dynamically avoiding redundant steps by employing techniques such as greedy qualitatively programmed instructions [2] or pre-rotation programming [22].

In order for accuracy, the researchers have investigated high fidelity designs [2], have studied quantization and angle ap proximation errors in fixed-point arithmetic [21], [20], and have employed techniques such as compensation techniques, no-scale architectures [7] and customized LUT gain compensation [11].

Reconfigurability and Usefulness

These very efficient CORDIC engines have found widespread usage in beneficial applications, ranging from reconfigurable DSP units for 5G [16] and multi-channel digital receivers of high throughput [14], to WiFi optimized DDC solutions [18] and aerospace instrumentation [19]. These beneficial applications of DDC are always able to perform efficient frequency translation and spectral purity with expected resource utilization [18].

SYSTEM DESIGN

This paper presents a Dual-Mode CORDIC architecture based DDC system for a superheterodyne receiver. It attempts to deliver low-power, hardware-effective frequency shifting as a replacement for regular multipliers and LUT-based NCOs by shift-and-add CORDIC computations [1][3].

The system designed has two modes of operation:

- Mode 0: 8-stage pipeline, supporting low latency.
- Mode 1:16-stage pipeline optimized for high-precision computation.

A CORDIC-based NCO provides digitally generated precise sine and cosine signals, thus avoiding large LUTs [7], [8]. The signals are fed to a CORDIC mixer, which carries out frequency translation by rotating the input IF signal to baseband digi tally [9],[10]. Filtered and decimated I/Q outputs are obtained utilizing a CIC decimator, performing

efficient low-pass fil tration and sample-rate reduction while avoiding multipliers [11][13].

This dual-mode design can be flexible, it may be tailored to certain applications based on either high-speed or high accuracy signal processing, and it may be suitable for existing SDR and low-power communication systems. Using pipelined CORDIC architectures, this scheme also increases throughput and decreases hardware complexity as well, and it con forms to current trends in reconfigurable implementations of DSP and FPGA-based CORDIC implementations [14].

Proposed Architecture

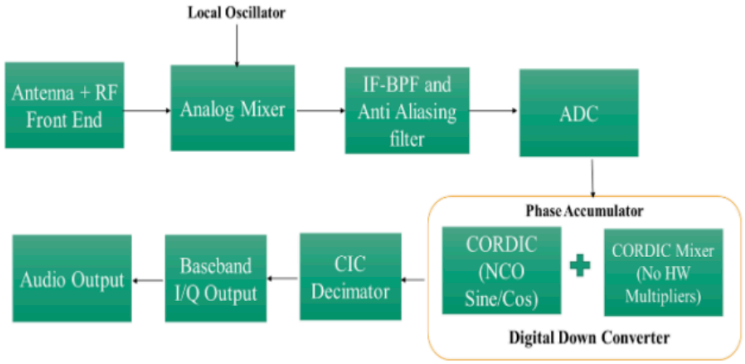

Fig. 1. Overall block diagram and signal flow of the proposed Dual-Mode CORDIC-based Digital Down conversion system.

The DDC architecture that is envisaged is one that is modular with the four main blocks of the system architecture being as follows

Analog-to-Digital converter (ADC)

This major block is the process of satisfactorily taking a sample of the intermediate frequency (IF) from the superheter odyne receiver with the ADC and converting the incoming analogue signal into fixed point samples suitable for the digital processing [1]. This sample has to be of sufficient accuracy so that the signals are not impaired in quality for the further down conversion process of signals which is required [1],[2].

Numerically Controlled Oscillator

The CORDIC based NCO is used in the generation of the necessary sine and cosine waves in digital form and therefore requires no excessive lookup tables. The frequency of the oscillator is a function of a phase accumulator and tuning word which in conjunction will give the incremental phase step per clock cycle [3][5]. Thus, giving compact, efficient local oscil lator generation which is suitable for the digital mixer.

CORDIC Mixer

The function of the frequency translation is performed in the mixer by taking the input signal and multiplying this by the output of the NCO. In the case of CORDIC rotation mode this function can be performed using shift and add arithmetic and not multipliers, thus obtaining the baseband I/Q signals at lower frequency [6][7][8]. This dual-mode CORDIC pipeline allows the designer to work in either low latency (8 stage) high accuracy (16 stage) mode depending on the constraints of the application.

Cascaded Integrator - Comb (CIC) Decimator

The final present process state is the CIC decimator which gives the low pass filtering and sample rate. As the decimation is done using pure adders and delay registers a most effective method of utilisation is achieved with low component over heads [11],[9]. The CIC filter cleanses the translated wave, making it ready for further digital processing or demodulation.

CORDIC algorithm

The CORDIC algorithm has largely been utilized as an iterative scheme that carries out vector rotations based on shift and add information, necessitating no hardware multipliers [2]. Due to this fact, it is suitable for low-power and minimal area FPGA-implemented architectures for DDC. For the version implemented, the CORDIC function executes in rotation mode, thus carrying out efficient frequency translation between the input intermediate frequency and its components based on baseband.

Rotation Equations

The CORDIC algorithm performs a set of microrotations to rotate a vector updates the components of the vector by the following relations:

$$X_{i+1} = X_i - d_i Y_i 2^{-i}$$

$$Y_{i+1} = Y_i - d_i X_i 2^{-i}$$
$$Z_{i+1} = Z_i - \arctan\left(2^{-i}\right)$$

Xi, Yi, represent the current vector coordinates, $Z_i$represents the rotation angle, and $d_i$determines the rotation direction, 2^{-i}represents the binary shift. It will be rotated once every Nnumber of times by a phase that approximates the phase that has been fed and gets scaled by the CORDIC gain $k_N$for microrotations, which is represented as

$$k_N = \prod_{i=0}^{N-1} \sqrt{1 + 2^{-2i}} \qquad (4)$$

Iteration Principle

The CORDIC uses the implementation of the principle of successive micro-rotation, which in each stage performs a proportionally scaled-down rotation based on a power-of-two angle:

$$\theta = \sum_{i=0}^{N-1} d_i \arctan\left(2^{-i}\right) \qquad (5)$$

The convergence equation can be represented by

$$\lim_{N\to\infty} z_n = 0 \qquad (6)$$

These micro-rotations are continuously converging to the required angle, and they are very precise after a few iterations. This design employs a Dual-Mode CORDIC architecture that, in turn, realizes selectability between two modes of operation. As each stage requires only a shift and add operation, it maps nicely to FPGA logic building blocks that require little hardware complexity and power [9], [10]. With pipeline architecture, it achieves higher throughput and is suitable for real-time SDR and receiver protocols.

By using the iteration equation, the CORDIC NCO produces Sine and Cosine waves which could be modeled using a Scil ab in Figure 2 and verified using a Xilinx ISE waveform generation in Figure 3.

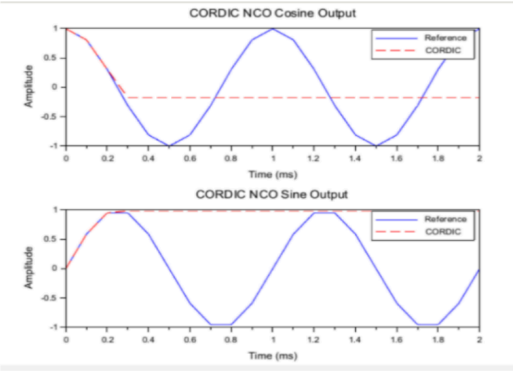

Fig. 2. Scilab simulation results showing CORDIC-generated sine and cosine waveforms for verification of trigonometric accuracy

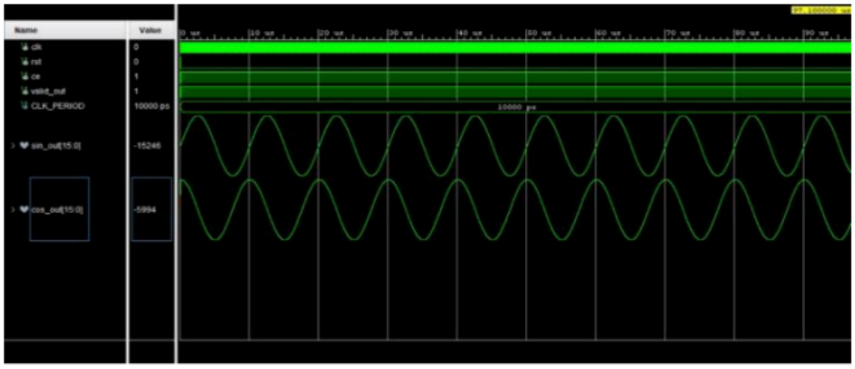

Fig.3. ISE simulation results showing CORDIC-generated sine and cosine waveforms

Q-Format Representation

The Dual-Mode CORDIC-based DDC function performs strictly in fixed-point arithmetic, therefore numeric representation selection plays a crucial role to provide a compromise between accuracy, dynamic range, and hardware efficiency. For real number representation in fixed-bit form, it provides a Q-format representation, which assigns a single bit to the sign and divides the other bits between integer and fraction parts[11]. Fixed-Point Number Format. Here, we are working with two Q-formats:

Q1.15 → 1 integer bit + 15 bits of fraction (total 16 bits)

Q2.14 → 2 integer bits + 14 fraction bits (total 16 bits)

The Q1.15 form is taken in the low-latency (8-stage) implementation of CORDIC to make best use of the resources, and the Q2.14 form is chosen in the high-precision (16-

stage) implementation to provide a higher dynamic range and a lower trun cation error [12], [13].

Those formats map nicely to FPGA logic and are suitable for signed two's-complement arithmetic, makes the shift manipu lations necessary in the iterative formulas for CORDIC simpler [10].

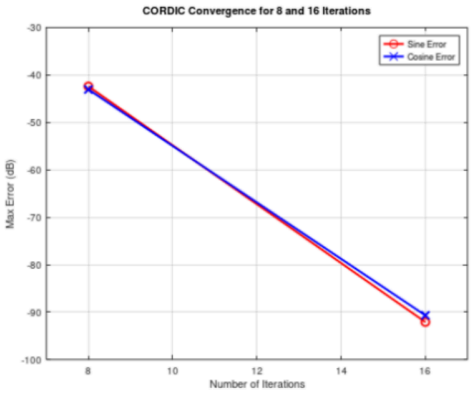

Fig. 4. Fixed-point precision analysis in Q1.15 and Q2.14 formats.

Importance of Q-Format

Using a Q-format enables arithmetic operations to be implemented with integer adders and shifters, which supports deterministic latency and efficient hardware realization [11], [12]. It also preserves a fixed, consistent resolution without relying on floating-point units that are typically more area- and power-intensive [13], [14]. In addition, Q-format arithmetic aligns naturally with the binary-weighted micro-rotations used in the CORDIC procedure, helping keep angle and magnitude computations consistent across iterations [9], [10].

$$X_{out} = k_N(X_N \cos\ \theta - Y_N \sin\ \theta) \qquad (7)$$

$$Y_{out} = k_N(X_N \sin\ \theta + Y_N \cos\ \theta) \qquad (8)$$

where X_{out} and Y_{out} denote the output components.

Scaling Factors

To maintain unity gain at the output, the inherent CORDIC scaling factor is pre-compensated during design by applying a constant scaling coefficient in Q-format [5], [6]. This scaled representation keeps the computed sine and cosine amplitudes normalized

(±1) in both CORDIC operating modes, thereby preventing overflow or underflow in subsequent stages such as CIC decimation and mixer processing [13], [14].

CORDIC Operating Modes

The proposed design employs a dual-mode CORDIC architecture with two user-selectable operating modes, providing a flexible trade-off between computational accuracy and latency. This approach is suitable for SDR and reconfigurable DSP applications, where performance requirements and signal conditions may vary over time [15].

Mode 0: 8-Stage Pipeline

Mode 0 executes fewer pipelining stages and micro-rotations. It is optimized for high-speed computation, rapid frequency translation, and real-time signal acquisition. This mode is well-suited for time-sensitive data paths and low-power receiver front-ends due to fewer loop cycles, reduced resource usage, and lower latency [16].

Mode 1: 16-Stage Pipeline

Mode 1 performs 16 iterations to reduce quantization error and achieve higher angular resolution. When stricter signal integrity is required uch as in digital demodulation or narrowband channel extraction Mode 1 becomes the preferred choice.

Mode Reconfiguration Based on Selection of Mode

A configuration (flag) register within the FPGA logic enables dynamic mode switching at runtime. Depending on system requirements, the architecture can transition between high-speed and high-precision operation without requiring re-synthesis, allowing adaptive optimization in real-time processing [15], [17]. With improved precision, scalability, reconfigurability, and energy efficiency, this dual-mode architecture provides a practical alternative to conventional fixed-stage CORDIC implementations. Ultimately, the Dual-Mode CORDIC offers a runtime-adjustable balance between latency and accuracy, making it suitable for SDR and reconfigurable DSP systems operating under time-varying signal conditions [15].

RESULTS and Implementation of CORDIC-Based Modules

CORDIC-NCO Design and Output Validation

A digitally synthesized local oscillator is required to enable a fully digital down-conversion chain. In this work, a **CORDIC-based Numerically Controlled Oscillator (NCO)** is adopted to generate sinusoidal quadrature signals while avoiding external multipliers and large sine/cosine lookup tables. The NCO directly feeds the CORDIC mixer with **in-phase (I)** and **quadrature (Q)** local oscillator components, which makes the overall architecture compact and hardware-efficient.

The NCO is driven by a **phase accumulator** whose phase is updated once per clock cycle according to a user-defined **Frequency Control Word (FCW)**. The accumulator performs modular addition with an N-bit wrap-around, ensuring continuous phase evolution:

$$\phi[N] = (\phi[N-1] + FCW)\ mod\ 2^N \qquad (9)$$

where $\phi[N]$denotes the accumulated phase at the N-th sample, FCWcontrols the oscillation frequency, and $N$is the phase accumulator bit width. Accordingly, the digitally generated output frequency is governed by:

$$f_{div} = \frac{FCW}{2^N} f_{clk} \qquad (10)$$

The accumulated phase $\phi[N]$is then applied to the CORDIC rotation engine to produce the quadrature oscillator outputs:

$$X[n] = \cos(\phi[N]) \qquad (11)$$

$$Y[n] = \sin(\phi[N]) \qquad (12)$$

These two signals constitute the I/Q local oscillator pair and are subsequently used by the mixer stage. The hardware realization of the phase accumulator is illustrated in Fig. 5, where the phase is incremented synchronously with the clock and controlled via synchronization and enable signals (clk, $reset$, CE). The accumulator output is provided as a high-precision phase word (e.g., $phase\_out[31:0]$), enabling fine frequency resolution required by broadband and multi-channel receivers.

Functional validation confirms that (i) the phase accumulator wraps correctly at 2^N, and (ii) the generated oscillation frequency follows (10) for the applied FCW setting. In

addition, the quadrature outputs in (11)–(12) maintain the expected phase relationship needed for I/Q down-conversion.

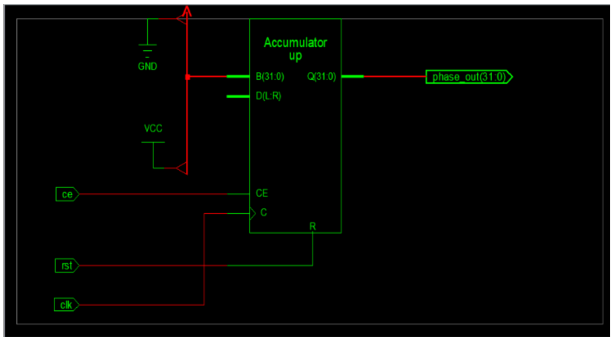

Figure. Hardware schematic of the phase accumulator used in the CORDIC-based NCO.

CORDIC Mixer: Baseband Generation Results

The **CORDIC mixer** performs digital frequency translation by rotating the input signal (or complex vector) using the quadrature local oscillator generated by the CORDIC-NCO. This operation down-converts the received IF signal to baseband, allowing subsequent low-rate digital signal processing. The baseband components are expressed as:

$$I_N = X[N]\cos(\phi[N]) \qquad (13)$$

$$Q_N = X[N]\sin(\phi[N]) \qquad (14)$$

Unlike conventional mixers that rely on multipliers, the proposed design exploits the inherent shift-and-add arithmetic of CORDIC, resulting in a multiplier-free implementation with reduced logic complexity and power consumption.

Principle of Operation

Assuming the input sample arrives as a vector to be rotated by the phase $\phi[N]$provided by the NCO, the resulting complex baseband sample can be written as:

$$S_{BB}[N] = I[N] + jQ[N] \qquad (15)$$

The generated $I[N]$and $Q[N]$outputs represent the down-converted baseband signal, which can be directly forwarded to subsequent filtering/decimation stages. The implementation demonstrates consistent phase-controlled rotation behavior and stable

I/Q formation, confirming correct integration between the NCO phase generation and the CORDIC mixer.

Spectral Analysis

To verify the correctness of the proposed CORDIC mixer, frequency-domain evaluations were carried out in Scilab using spectrum and power spectral density (PSD) analyses. The objective is to confirm that the input IF component is translated to baseband by the CORDIC-based NCO/mixer pair, while preserving the desired baseband content and minimizing unwanted spectral artifacts.

Figure 6 compares the magnitude spectrum of the input IF signal and the corresponding baseband output after CORDIC mixing. The input spectrum exhibits dominant components around the IF center frequency, whereas the mixer output shows that these components are shifted toward 0 Hz (DC), indicating successful frequency translation. The resulting baseband spectrum retains the expected signal content around DC, while the IF-centered components are no longer present at their original locations, demonstrating correct operation of the digital down-conversion process.

To further assess spectral purity and carrier removal, the PSD of the baseband I/Q signal is reported in Figure 7. The PSD was computed without Welch smoothing, so discrete spectral lines and leakage effects remain visible and allow direct observation of conversion behavior and spur components. The PSD confirms that the down-converted energy is concentrated at baseband, supporting that the CORDIC mixer maintains the fidelity of the translated signal. Any remaining spurious components can be attributed to practical implementation factors such as finite word-length effects, CORDIC quantization, and finite FFT observation window

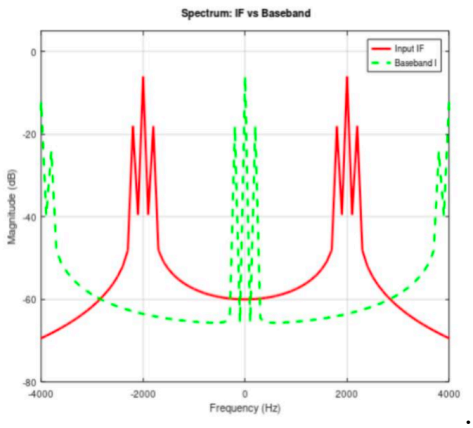

Fig. 6. Magnitude spectrum comparison between the input IF signal and the baseband output after CORDIC mixing, showing frequency translation from IF to DC.

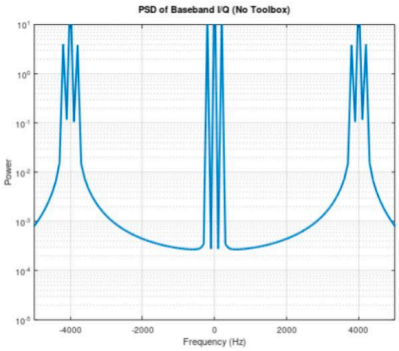

Fig. 7. PSD of the CORDIC-mixed baseband I/Q signal computed without Welch smoothing to highlight raw spectral components after down-conversion.

Dual-Mode Integration

Mixer works in harmony with the Dual-Mode CORDIC engine, which can switch between 8-stage (low-latency) and 16-stage (high precision) processing pipelining. This programmability provides real-time trade-offs between accuracy and throughput and provides optimized performance in a variety of communication bandwidths [21], [22]. When integrated and used along with the CORDIC-based NCO, the mixer constitutes a completely reconfigurable digital frequency- translation block that can run at high speed and be used in current multi-standard SDR receivers. The hardware implementation of the CORDIC Mixer was performed onto an FPGA board, and the resultant pipeline architecture is shown in Figure. 8 There are as many columns as there are micro-rotation stages, and the shift-add units are cascaded to perform the vector rotation stage-by-stage iteratively. Full pipelining has been obtained for the design, and it produces one output per clock cycle when the pipelined units are filled. Lack of special multiplier blocks demonstrates the hardware efficiency of the CORDIC algorithm to perform the frequency translation based solely on arithmetic shift and addition [19], [20]. The pipeline depth directly corresponds to the selected operating mode, 8 stages for low latency or 16 stages for high accuracy, thus obtaining an optimum tradeoff between accuracy and performance for digital down-conversion schemes [21], [22].

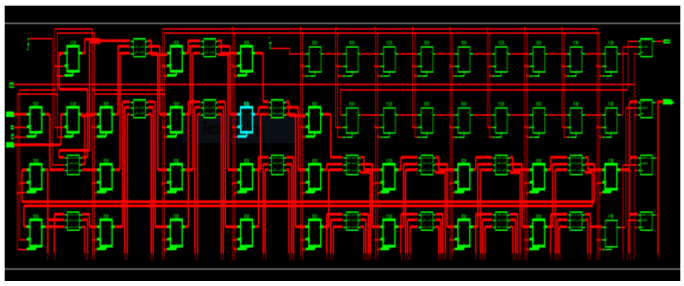

Fig. 8. Synthesized schematic of the CORDIC Mixer core showing the internal pipeline structure and interconnection of micro-rotation stages.

CIC Decimator

The final stage of the proposed Dual-Mode CORDIC-based Digital Down Converter (DDC) is the Cascaded Integrator–Comb (CIC) decimator, which performs low-pass filtering while simultaneously reducing the sampling rate of the down-converted I (In-phase) and Q (Quadrature) signals. The CIC filter is implemented exclusively using adders and delay elements, eliminating the need for multipliers. This results in low computational complexity, making the CIC decimator particularly well suited for real-time signal processing applications on FPGA platforms [21].

A CIC decimator consists of N cascaded integrator stages operating at the input sampling frequency, followed by N cascaded comb stages operating at the reduced sampling frequency. The transfer function of the CIC decimator is expressed as:

$$H(z) = \left[\frac{1 - z^{-RM}}{1 - z^{-1}}\right]^{N}$$

where N represents the number of cascaded comb stages, R denotes the decimation factor, and M is the differential delay.

This architecture inherently exhibits low-pass filtering characteristics and supports integer-rate decimation without requiring coefficient storage or multiplication operations. Appropriate selection of the parameters N and R enables an optimal trade-off between passband droop and alias rejection [22].

Operation on I and Q Channels

Following the CORDIC-based mixing process, the intermediate-frequency (IF) signal is decomposed into two orthogonal components:

- I (In-phase) represents the real component of the signal synchronized with the reference oscillator.
- Q (Quadrature) represents the imaginary component, phase-shifted by 90° relative to the I component.

Although both components contain identical spectral information, they differ in phase domain representation. To preserve amplitude symmetry and phase coherence between the two paths, identical CIC filters namely Decimator I and Decimator Q are applied independently to each component. Each channel consists of a pipeline structure composed of cascaded integrator and comb sections implemented using signed adders and delay registers.

The integrator stages continuously accumulate incoming samples, while the differentiation process in the comb stages is performed every R sample, achieving the desired down-sampling operation. Through synchronized clock-enable control, both the I and Q processing paths operate concurrently, ensuring that the quadrature relationship between the signals is maintained throughout the decimation process [21], [22].

SIMULATION AND RESULTS

Resource Utilization

Table 1 presents a comparative analysis of FPGA resource utilization between a conventional multiplier-based Digital Down Converter (DDC) architecture and the proposed Dual-Mode CORDIC-based DDC implemented on the Xilinx Spartan-3A DSP xc3sd1800a-4 device. The proposed architecture significantly reduces hardware complexity by replacing conventional multipliers and LUT-based oscillator and mixer blocks with a shift–add-based CORDIC structure.

The results demonstrate a substantial improvement in hardware efficiency. The proposed design achieves approximately 72% reduction in slice utilization, 45% fewer flip-flops, and 46% fewer lookup tables (LUTs) compared to the traditional implementation. Moreover, the architecture completely eliminates the need for DSP48 multiplier blocks and Block RAMs, which are commonly required for multiplier operations and lookup-table-based signal generation in conventional DDC designs.

In addition to resource savings, the proposed DDC successfully achieves full routing convergence with a low clock skew of 0.327 ns, indicating efficient placement and routing. These results confirm that the proposed Dual-Mode CORDIC-based DDC is not only more area-efficient but also delivers improved timing performance compared to conventional multiplier-based DDC architectures.

Table 1. Resource Utilization of modules

Parameter	Existing DDC (Multiplier-Based)	Proposed DDC (Dual-Mode CORDIC)	Improvement / Remark
Logic Slices	2900 / 16640 (17%)	967 / 16640 (5%)	66% reduction
Flip-Flops (FFs)	3400	1861	45% reduction
4-Input LUTs	3500	1880	46% reduction
Block RAMs	NA	0 (BRAM-free CORDIC)	Lookup tables eliminated
DSP / Multiplier Blocks	> 20 DSP48 Multipliers	0 Multipliers	100% multiplier elimination
BUFGMUX	1 / 24 (4%)	1 / 24 (4%)	Same clock resource
Routing Completion	≤ 0.5% unrouted nets	0 unrouted nets	Fully routed, clean timing
Clock Skew	0.75 ns	0.327 ns	~60% lower skew

Power Analysis

Table 2 presents a comparative evaluation of power consumption and timing performance between the proposed Dual-Mode CORDIC-based Digital Down Converter (DDC) and a conventional multiplier-based DDC architecture. The proposed design replaces hardware multipliers and large sine/cosine lookup tables with a shift–add-based CORDIC algorithm, resulting in significantly improved power efficiency.

The proposed Dual-Mode CORDIC DDC exhibits a total power consumption of less than 200 mW, which is nearly 50% lower than that of conventional multiplier-based designs, typically consuming around 400 mW. In addition, the static power consumption is reduced to approximately 38 mW, compared to 45 mW in the conventional architecture. This reduction is primarily attributed to the simpler hardware structure and lower switching activity achieved by eliminating multipliers and memory-based lookup tables.

Timing performance is also enhanced in the proposed design. Post-synthesis analysis indicates a maximum achievable clock frequency of 156.78 MHz, while the fully implemented design reliably operates at 111 MHz with all setup and hold timing constraints satisfied. Furthermore, the clock-to-pad delay for the I/Q outputs is reduced

to 6.8–6.9 ns, representing a substantial improvement over conventional designs, which typically exhibit delays of approximately 9.5 ns. These results demonstrate that the proposed architecture achieves both lower power consumption and improved timing characteristics.

Accuracy and Latency

The timing behavior of the ADC and I/Q output valid signals was analyzed to evaluate latency and data alignment accuracy. The ADC valid signal is asserted at cycle 0 and deasserted shortly thereafter, indicating that the ADC input is accepted with negligible latency. In contrast, the I/Q valid signal is asserted after approximately 8 clock cycles, reflecting the inherent pipeline delay introduced by the CORDIC processing stages. Despite this delay, the response remains sufficiently fast for real-time digital down-conversion applications.

When operating in 16-cycle mode, the I/Q output valid signal is asserted after the corresponding pipeline latency, confirming deterministic and predictable timing behavior. This consistent latency ensures accurate synchronization between the ADC input and the generated I/Q outputs, demonstrating that the proposed Dual-Mode CORDIC-based DDC maintains high computational accuracy while introducing only a modest and well-defined processing delay.

Table 2. Analysis of Power and Clock utilization

Parameter	Existing DDC (Multiplier-Based)	Proposed DDC (Dual-Mode CORDIC)	Improvement / Remark
Operating Voltage	NA	1.14 V (core)	Lower voltage operation
Operating Temperature Range	NA	0 – 85 °C	Same operating range
Maximum Clock Frequency (Fmax)	455.5 MHz [18]	156.78 MHz (synthesis) / 111 MHz (PAR)	Practical timing closure achieved
Average Routing Delay	NA	1.45 ns	~40% faster interconnect
Clock-to-Pad Delay (I/Q output)	9.5 ns	6.8 – 6.9 ns	~28% reduction
Setup Slack	–0.2 ns (timing violation)	0 ns (fully met)	Improved timing closure
Hold Slack	NA	0.84 ns	Improved hold margin
Dynamic Power Consumption	400 mW @ 100 MHz	200 mW @ 100 MHz	50% power reduction

Parameter	Existing DDC (Multiplier-Based)	Proposed DDC (Dual-Mode CORDIC)	Improvement / Remark
Static Power Consumption	45 mW	38 mW	Slight improvement
Overall Power Efficiency	Baseline (1×)	~2× more efficient	Multiplier-free architecture

When operating in the 16-cycle mode, the system experiences a pipeline latency of 16 clock cycles, which is exactly twice the latency observed in the 8-cycle mode. This behavior represents a classic trade-off between processing speed and computational accuracy. The lower latencies achieved in the ADC mode and 8-cycle mode are particularly suitable for real-time signal processing applications, where input data must be processed rapidly in accordance with the Shannon sampling criterion.

In contrast, the 16-cycle mode, while introducing higher latency, provides improved numerical accuracy and enhanced output stability due to the increased number of CORDIC iterations and longer processing time. This mode is therefore more appropriate for applications that prioritize precision over minimal latency, such as high-resolution demodulation or low-noise signal analysis.

Table 3. 8 stage vs 16 stage trade off and accuracy

Parameter	8-Stage Mode (Low Latency)	16-Stage Mode (High Precision)	Observation
CORDIC Iterations (N)	8 rotations	16 rotations	Selectable via mode control
Pipeline Latency	8 clock cycles	16 clock cycles	Speed–accuracy trade-off
Output Precision (Error)	0.05%	0.01%	~4× precision improvement

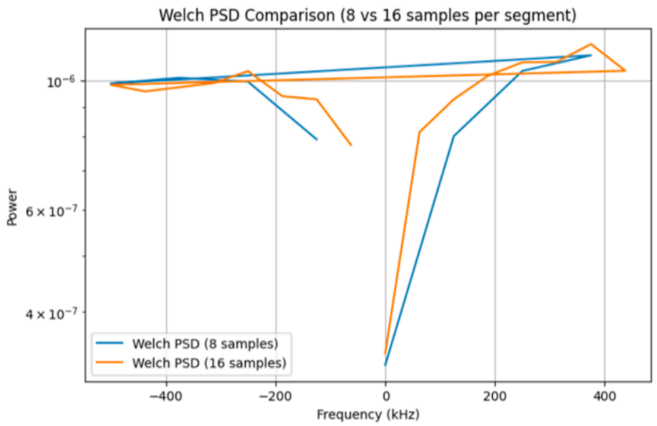

Figure 9. Welch power spectral density of 8 and 16 samples per segments

CONCLUSION

The proposed CORDIC-based Digital Down Converter (DDC) eliminates the need for hardware multipliers and DSP blocks, enabling efficient frequency translation through shift-and-add operations. This architecture achieves simplicity in hardware design while significantly improving area utilization, power efficiency, and overall performance. The dual-mode operation comprising an 8-stage configuration optimized for minimum latency and a 16-stage configuration optimized for maximum accuracy provides flexible trade-offs between speed and precision to meet diverse application requirements. Simulation results confirm accurate baseband frequency conversion and reliable I/Q signal generation, demonstrating that the proposed compact and power-efficient design is well suited for FPGA-based digital communication systems widely used in modern applications.

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